REMARKS

Reconsideration and allowance of the subject application are respectfully requested. Claims 1-21 are all the claims pending in the application, as claims 18-21 are hereby added. Applicant respectfully submits the pending claims define patentable subject matter.

Claim Rejections - 35 USC § 112

Claims 2 and 12 remain rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

In the Amendment filed April 10, 2007, Applicant argued claim 2 is enabled by the Specification. In particular, Applicant argued the data and meta-data information could, for example, be written at different times if the main area of the block and the spare area of the block are physically separate blocks, each capable of being written to at different times.

However, the Examiner disagrees and asserts the Specification does not teach how the main area of a block and the spare area of the block are physically separate blocks. The Examiner further contends this interpretation is inconsistent with the language of the claims. Citing claim 1, the Examiner argues since "the flash memory controller is configured to write data and meta-information in a physical block," the Specification does not enable one of ordinary skill in the art to write the data and meta-information in physically separate blocks. The Examiner alleges paragraph [05] of the Specification discloses the block is the unit of data that can be read or written in a read or write operation. Applicant respectfully disagrees with the Examiner's rationale.

FIG. 4 shows a block of the NAND-type flash memory 100. Paragraph [51] discloses block 100 comprises:

> a main area 110 and a spare area 130. Data are stored in the main area 110 and meta-information of the relevant block is stored in the spare area 130.

Thus, in the exemplary embodiment of Fig. 4, the memory has two parts, the main area 110, and the spare area. Consequently, a write operation could exist which writes data and meta-information to the main area 110 and the spare area 130, respectively. Thus, Applicant submits one skilled in the art would understand such a write operation could involve writing one value first, e.g., data in the main area 110, and then the second value, e.g., the meta-information in the spare area 130.

In view of the above, Applicant submits claims 2 and 12 comply with the enablement requirement of 35 U.S.C. § 112, and therefore, Applicant respectfully requests the Examiner reconsider and withdraw the rejection.

Claim Rejections - 35 USC § 102

Claims 1, 3-4, 11 and 13-14 remain rejected under 35 U.S.C. 102(b) as being anticipated by Conley (U.S. Pat. App. Pub. No. 2002/0099904). Applicant submits the rejection is improper.

In response to our arguments submitted in the Amendment filed April 10, 2007, the Examiner states:

> Claim 1 recites "the flash memory is configured to perform a write operation for writing the data and the meta-information allocated to the logical block in a new physical block without changing flash memory state information written in a previous physical block corresponding to the logical block if the previous write operation has been performed for the logical block". This limitation, given broadest reasonable interpretation, requires that flash memory state information written in a previous physical block is not changed. If there is no flash memory state information written in a previous block, there is no flash memory state information to change, and therefore it is not possible for the

> controller to change flash memory state information written in the previous physical block. Accordingly, if there is no flash memory state information written in a previous block of Conley, there is no flash memory state information to change, and therefore, the system of Conley would write the data and meta-information in a new physical block without changing flash memory state information written in a previous physical block.

Applicant respectfully disagrees with the Examiner's position.

Independent claim 1 specifically requires, *inter alia*, the flash memory controller "perform a write operation for writing the data and the meta-information ... in a new physical block without changing flash memory state information written in a previous physical block[.]"[1] Since the claim requires the operation to be performed without changing information written in a previous physical block, it is inherent that information has previously been written in the previous physical block.

Thus, it is illogical to say if flash memory state information is not written in a previous block in Conley, then Conley would write the data and meta-information in a new physical block without changing flash memory state information written in a previous physical block. That is, if flash memory state information is not written in a previous block of Conley, as the Examiner asserts, then it does not follow that Conley would write to a new physical block without changing the flash memory state information which is written in the very same previous physical block assumed not to have anything written in it.

The Examiner further states:

> Applicant is encouraged to amend independent claims 1 and 11 to positively recite that written blocks contain flash memory state

[1] Emphasis added.

> information, to clarify that the claims require flash memory state information, if that is the intended scope of the claims.

However, Applicant notes the claim already requires flash memory state information. As noted above, independent claim 1 recites, in part, "without changing flash memory state information written in a previous physical block." Thus, the claimed invention expressly requires, *inter alia*, the operation to be performed without changing the flash memory state information, which has already been written, i.e., presently existing, in previous physical block.

Moreover, as noted previously, Conley merely discloses a physical block[2] having a logical block number[3] and a time stamp.[4] The time stamp used in Conley simply indicates the time data was last written to the physical block. A time stamp is different from state information since a time stamp indicates time, whereas state information indicates a status.

Further, Conley fails to discuss state information, i.e., a status of the physical block itself. Since the claimed invention requires, *inter alia*, flash memory state information written in a previous physical block, Applicant submits Conley does not teach or suggest the feature "without changing flash memory state information written in a previous physical block," as claimed.

Accordingly, Applicant submits independent claim 1 is patentable over Conley for at least these reasons. Similarly, Applicant submits independent claim 11 is patentable over Conley for reasons analogous to those stated above regarding claim 1. Further, Applicant submits claims 3, 4, 13 and 14 are patentable over Conley, at least by virtue of their dependency.

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[2] See e.g., Conley, FIG. 8, element 35.

[3] See e.g., Conley, FIG. 8, element 41.

[4] See e.g., Conley, FIG. 8, element 43.

Claim Rejections - 35 USC § 103

Claims 5-6, 8-10, 15 and 17 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Conley in view of Kim et al. (U.S. Pat. No. 6,381, 176; hereinafter "Kim"). Applicant respectfully traverses the rejection.

Applicant submits Kim does not cure the deficiency of Conley noted above. Thus, Applicant submits none of the cited references, either alone or in combination, teaches or suggests all of the claimed features of independent claims 1 and 11. As such, Applicant submits claims 5, 6, 8-10, 15 and 17 are patentable over the cited references, at least by virtue of their respective dependency on claims 1 and 11.

New Claims

Applicant herein adds new claims 18-21. No new matter has been added. Applicant submits independent claim 18 is patentable over the prior art of record for reasons analogous to those stated above regarding independent claim 1. Further, Applicant submits new claims 19-21 are patentable over the prior art of record, at least by virtue of their respective dependency on claim 18.

Amendment to Independent Claim 11

Applicant herein amends independent claim 11 to correct a minor typographical error.

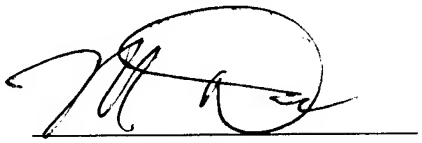
Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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